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All Digital Spread Spectrum Clock Generator For Fast Prototyping

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ABSTRACT

The spread spectrum clock generator produces frequency modulated clock signal with varying period. Spread spectrum clock is used instead of fixed frequency clock signal in digital circuits to reduce the EMI noise generated by clock. Available SSCG designs uses complex modulation control techniques leading to high power consumption. Implementation of complex SSCG design in FPGA during prototype stage will increase the time-to-market of digital systems with SSC. This project presents a full digital spread spectrum clock generator design built by leveraging Digital Phase Locked Loop design. The presented SSCG design is simple and implementation in FPGA is quick due to use of predesigned library modules. A counter based digitally controlled oscillator setup is used to minimize power and complexity. The complete design is implemented using HDL and synthesized. The proposed design shows reduced power consumption compared to existing design

Keywords
Digital Spread Spectrum Clock Generator, Electro Magnetic Interference (EMI) reduction, Digital Control Oscillator (DCO), ALL Digital Phase Locked Loop (ADPLL), ease of prototype

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Introduction

The advancement of digital designs for more processing speed have exponentially increased the system complexity and signal speed. This has led to the use of high-speed switching signals, with high harmonics that causes Electro Magnetic Interference (EMI) noise. Due to the destructive nature of EMI, various techniques like shielding, slow signal transition, signal filters and Spread Spectrum Clock Generator (SSCG) are used for controlling its generation. Among all EMI reduction techniques, SSCG has the advantage of low cost, efficient area and optimal performance.

As digital systems have become streamlined, reducing the prototyping and development period of the system is important for product developers. The existing SSCG designs have complex controllers and PLL blocks that must be separately modelled. This is not ideal for use in prototype stage. Also, it is difficult to design timing paths in circuits with SSC and non-SSC clocks, if SSCG is not present in the prototype stage of the circuit. This requirement creates the need for a simple, flexible, completely digital SSCG model that can be designed and implemented rapidly in FPGA during the prototype stage to improve the quality of end product without delaying the time-to-market.

A completely digital and synthesizable SSCG design is proposed in [1], [2] and [6], but the Digital Controlled Oscillator (DCO) used in these designs are based on digital delay lines and delta-sigma modulation. For quick implementation, digital delay line and delta-sigma modulation is not feasible due to its complexity. Existing digital SSCGs are built upon a basic Phase Locked Loop (PLL) that must be designed separately. This adds to the design time and not useful in prototyping. The All Digital Phase Locked Loop (ADPLL) design in [5] presents a counter based DCO that can be used for prototype SSCG design. A digital SSCG ideal for prototype stage is designed by borrowing the DCO architecture in [5] and facilitating the quick implementation of base PLL using schematic design like in [7].

The rest of the paper is organized into three sections. The proposed SSCG design architecture and working is presented in Section II, experimental results obtained are reported in Section III and derived conclusion is discussed in Section IV.

Proposed Digital Sscgdesign

A.digital sscg architecture overview

The proposed SSCG design is targeted towards prototyping ease and rapid implementation. The design is based on digital PLL model, which is altered to include a SSCG controller to modulate the output clock signal. The overall function of PLL is the same, there is a Phase Detector that generates the phase difference between reference and feedback signal, the generated phase difference is decoded into a digital code which is provided to the DCO to form clock signal with the required phase fix. The overall block diagram of the proposed design is shown in Fig. 1. A center spread modulation based on triangular envelop is considered in the proposed model due to its simple and efficient design. The proposed design can work as a normal PLL or SSCG with respect to the select bit MODE. If MODE = 0, the DCO generates constant clock signal, if MODE = 1, modulated digital code is selected. The change between PLL and SSCG is controlled by a 2-1 MUX. For incorporating the modulation part to the PLL design, a controller block is added, which varies the digital code (from digital filter to DCO input) with respect to the modulation value that can be programmed by the designer.

The digital PLL design used in this model can be implemented in schematic form using readily available modules in ISE Design Tool, Xilinx. This helps to improve

the implementation time during prototyping. The SSCG controller can be programed with required modulation parameters and added to the base PLL design to complete the SSCG. The crucial DCO can also be implemented with two existing modules from ISE Tool Library. The proposed DCO implementation reduces the complexity of delay line based DCO. One disadvantage of the proposed method is its low accuracy compared to delay line based SSCG design. But the proposed design will have necessary accuracy margin required in development stage.

The existing DCO architecture [6] uses delta sigma modulation technique to generate the input DCO code and digital delay line setup involving two stages of tuning. The delay line is built up of NAND gates and MUXs connected in series to the degree of code size. But the proposed DCO involves counters and an arithmetic unit, this reduces the design complexity.

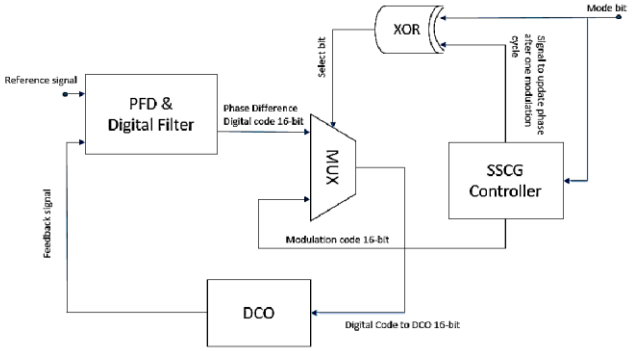

Fig. 1. Proposed Digital SSCG Block Diagram.

B.Application of proposed design

Due to the simple design, implementation of the proposed circuit during prototype stage will be easy. This advantage helps in reducing the prototype time for digital systems with EMI control requirement, as well as provides a better quality end design as the prototype can be designed with actual spread spectrum clock. The mentioned advantages will be useful in digital consumer product market as the need for these systems are facilitated by Internet of Things (IoT) and various automation applications.

C.Phase detector and Digital Filter

A D flip-flop-based PFD architecture is used in the proposed design. The PFD along with Digital Loop Filter module generates a 16-bit binary code of the phase or frequency difference. The Fig. 2 shows the PFD setup with D1 and D2 as the flops. Here, the D input of the flops are tied to a constant logic "1". The reference clock (Fref) and feedback clock (Ffed) signals are given to the clock pins of the flops. The AND gate gives logic "1" to clear the flops if both D1 and D2 outputs are high. The XOR gate output is used to control the digital integrator.

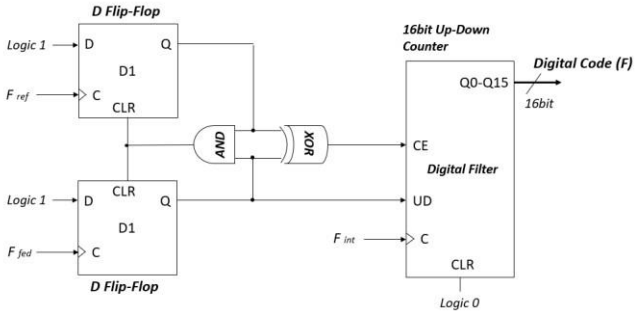

Fig. 2. Proposed DCO Logic Diagram.

For the Digital Loop Filter or integrator, a 16-bit up-down counter is used, which has an enable pin (CE) to start (when CE = 1) or stop (when CE = 0) the counter, this is shown in Fig 3.8. The UD pin decides whether the counter must count UP (when UD = 1) or Down (when UD = 0). The digital integrator is clocked (integrator frequency Fint) at the same frequency of the reference signal frequency (Fref = Fint). The XOR will give a logic "1" when there is a phase difference, which triggers the integrator to start counting. The UD signal is taken from the output of D2, so that if D2 is triggered first i.e.feedback signal leads reference signal, count will be incremental and if reference signal leads, count will be detrimental. The final digital code generated by the counter will be the required phase adjustment in the generated clock by the DCO.

D.Digital Controlled Oscillator

The DCO used in proposed design employs a counterbased model and archives the functionality of digital divider using an arithmetic unit and a T flip-flop. The counter is a 16bit resettable up counter, its output is provided to second input of a binary subtractor as shown in Fig. 3. The 16-bit binary code to the first input of the subtractor is from the digital filter. The binary subtractor has a borrow value output, this borrow value will be "1" (OV) when B is greater than A. The borrow value is used to reset the counter so that the counter will be repeatedly counting to the phase digital code value from filter. The borrow value is also given to a T flipflop, which generates a periodic signal with the binary code F as its pulse width. The counter and T flip-flops are controlled by a clock (count clk) that is ten times in frequency of the reference signal or integrator frequency.

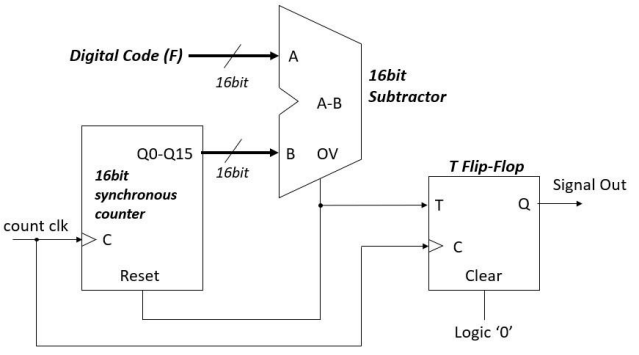

Fig. 3. Proposed DCO Logic Diagram.

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E.SSCG Controller

The Proposed SSCG controller is used to generate digital code value to the DCO when the design is in SSCG mode instead of digital filter. The controller takes the phase difference and the DCO counter value as inputs and generates a modulated pulse width value that is given to the DCO to create frequency modulated signal. The design of the controller uses a triangular modulation model like [6]. The working of the controller is shown in below Fig. 4. The controller uses user defined spread step value to reduce the signal width and generates a 1-bit signal after every cycle of modulation to re lock the output frequency with respect to the reference. The same signal is used to generate the select bit for the MUX that choose between digital filter output and controller modulated digital code output.

For triangular modulation, the controller decreases the period of the output clock from T flip-flop to the minimum possible value without going less than the slowest clock in the design. The minimum limit is followed to make sure no errors due to different clock frequency occurs. In modulation the DCO gets the input from the SSCG controller through the select MUX and the counter in DCO counts till the digital code value and toggling the T flip-flop output at every digital count threshold and reset. This process generates a single modulation cycle and then for one reference signal cycle the design works in PLL mode and repeats the modulation cycle.

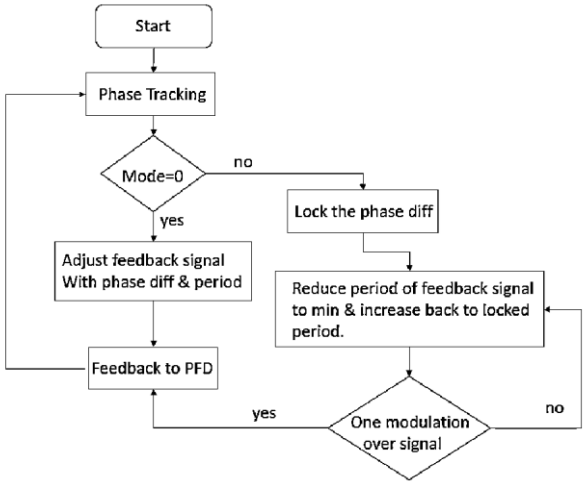


Fig. 4. Flowchart of SSCG Controller.

The spread ratio (SRT) of the generated SSC frequency depends on the defined modulation value. The triangular modulation is controlled by two parameters defined in SSCG controller, spreading range (SR) and spreading step (SS).

SRT = [SS * D * SR / 2] / TF

SS is the value by which the frequency is varied at each cycle, it is the resolution of modulation. SR is the number of steps in a single modulation cycle. These values can be programmed into the controller and the SRT can be determined using (1). D is the least delay of DCO in each step and TF is the fundamental period of the DCO signal

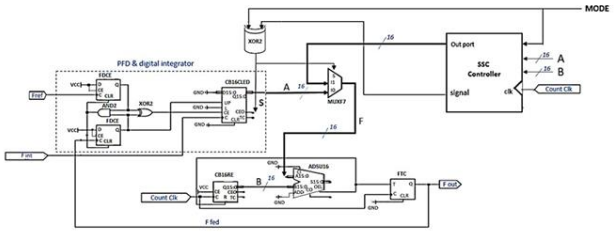


Fig. 5.Proposed SSCG with Library Modules

Implementation And Results

A.Implementation of Proposed Digital SSCG

The Xilinx Design Suite provides a set of standard functional modules that are pre elaborated, this can be used to implement the counters, ALUs and flip-flops in the design. Using the modules from Xilinx Schematic reduces the implementation time of SSCG, which is an advantage as this makes the prototyping of the SSCG simple.

TABLE I. SCHEMATIC EQUIVALENT OF FUNCTIONAL MODULES

Name of Component	**Schematic Label**
AND gate	AND2
XOR gate	XOR2
D Flip-Flop	FDCE
T Flip-Flop	FTC
2-1 Multiplexer	MUXF7
Digital Filter Counter 16-bit	CB16CLED
DCO Counter 16-bit	CB16RE
Subtractor 16-bit	ADSU16

The SSCG design implemented using readily available functional modules as per Table I is shown in Fig. 5. Unused pins in the modules are tied to VCC (logic 1) or GND (logic 0) to disable its function. The SSCG controller block consist of MUXs and standard gates that can be replaced by the schematic modules from the Table I.

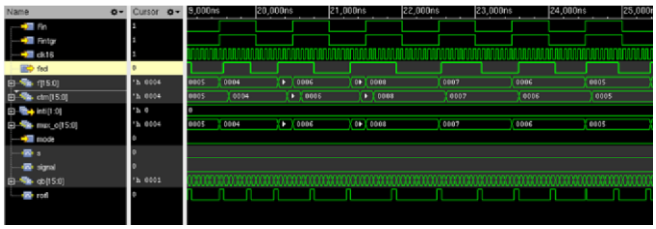
B.Expiremental Results

The proposed digital SSCG design is simulated in Cadence NC Launch Simulation GUI. The test simulation is run with reference and integrator frequency at 1MHz and DCOCounter Clock at 16MHz. Simulation of the digital SSCG is done in both PLL mode and SSCG mode.

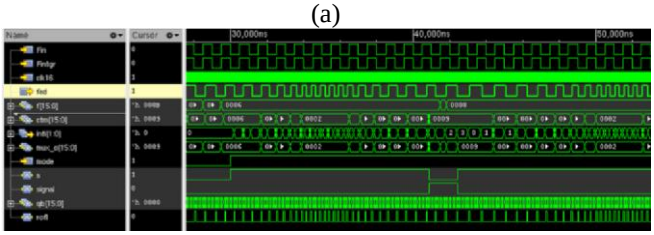
- The simulation result shown in Fig. 6(a) is with **mode** = 0, periodic clock signal is generated through **fed** pin with constant frequency (1MHz). Here the design acts like a PLL that generates output clock signal with reference frequency. The MUX will give the signal from digital filter as the output and the counter counts the till that value before resetting. The **signal** from controller will be always 0 as the design is in PLL mode. **F[15:0]** pin value keeps varying to adjust the phase difference between **fed** and **Fin.**

• When **mode** = 1, the design functions as a SSCG. The modulated digital code value from controller is from **ctm [15:0]**. The signal **inti [1:0]** indicates the change of step in modulation cycle. The modulated clock signal generated from output of T flip-flop is shown in Fig. 6(b). The output signal is produced from **fed** pin. After every modulation cycle the **signal** is set to logic 1, this makes the working to go back to PLL mode for a signal period of the reference signal. During this period, the phase difference in output with respect to the reference signal is adjusted. The MUX will select the output from controller to propagate to the ALU so that the DCO counter will count till the modulated digital code value.

The total power consumed by the proposed design at 270MHz maximum frequency is calculated using Encounter RTL Compiler for 90 nm process. Table II shows total power consumed proposed design and compares with other existing designs. The instance sscg is the top module and the total power is 0.346 mW. The power consumption of the proposed design is comparable to previous digital SSCG design [6], which uses similar triangular modulation and has a power value of 0.443 mW at 270MHz frequency and 90 nm process. The synthesized netlist area of the design is 4.35 mm², this can be further reduced by manual placement in physical design.



(a)



(b)

Fig. 6.Simulation Result (a) Functioning as PLL, (b) Functioning as SSCG.

The comparison of area and power of the proposed design with respect to existing designs with different modulation methods is shown in Table II. The area of existing designs are calculated in terms oof chip area while proposed design area is in terms of synthesized netlist.

TABLE II. PERFORMANCE COMPARISON

Performance Indices	**TCAS2 2011 [4]**	**JSSC 2010 [3]**	**TVLSIS 2014 [6]**	**Proposed**
Process	0.18µm	65nm	90nm	90nm
Modulation Method	Voltage Control Oscillator	Digital Delay-Line	Delta-Sigma	Counter Based DCO
Modulation Profile	Triangular	Arbitrary	Triangular	Triangular
Output Frequency (MHz)	162~270	180~1270	270	270
Power consumption (mW)	19 @ 270MHz	44 @ 1270MHz *	0.443 @ 270MHz	0.346 @ 270MHz

*: without PLL

Conclusion

The Proposed digital SSCG design is flexible and completely synthesizable. The simplicity and ease of implementation of the proposed design makes it a perfect choice for use in prototype stage of digital circuit design involving spread spectrum clock. This solves the redesign time and work required to change already finished digital circuit to include spread spectrum clock in later stages to reduce EMI. From area and power results it is clear that the digital SSCG design demonstrated in this project utilizes a small area in FPGA and has comparatively less power consumption to previously existing design. This counter based DCO design has less accuracy than delay line based DCO SSCGs, but provides enough resolution required in prototype stage. The design provides more control for the user to adjust the spread ratio of generated spread spectrum clock and mode of operation by using programmable SSCG controller.

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